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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,443	05/15/2006	Hideaki Kuwabara	740756-2969	7846

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

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12/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,443	KUWABARA ET AL.	
	Examiner	Art Unit	
	SCOTT R. WILSON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *1-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/15/06, 7/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 19-29 in the response filed 8/25/2008 is acknowledged.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: METHOD OF FORMING LARGE AREA DISPLAY WIRING BY DROPLET DISCHARGE.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 19-21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al. (US 6,952,036). As to claim 19, Suzuki et al., Figures 3(a) to 3(f) and 4(a) to 4(d), discloses a method for manufacturing a semiconductor device comprising the steps of: forming a base film (41)(col. 8, line 3) over a substrate (10)(col. 7, line 65) having an insulating surface; forming an insulating film (42)(col. 8, line 10)) over the substrate; forming a mask (col. 8, line 21) over the insulating film; forming a depression

(43) by selectively etching the insulating film (col. 8, lines 19-22), and forming an embedded wiring, embodied initially as layer (44a), in the depression by “any known technique” (col. 8, lines 64-65). Since the disclosed electroless plating technique of Suzuki et al. uses metal in a liquid solution, it may be performed by a droplet discharge method. See, for example, Kobayashi. Suzuki et al. further discloses removing the mask; performing a planarization processing (col. 9, lines 28-30) to an upper surface of the embedded wiring; forming a gate insulating film (47)(col. 9, line 67) over the embedded wiring; and forming a semiconductor film (active layer (50), which is the same as active layer (17)(col. 5, lines 56-57)) over the gate insulating film.

As to claim 20, Suzuki et al. discloses (col. 8, lines 21-23) that the base layer (41) is used as an etching stopper in the step of forming the depression by selectively etching the insulating film (42).

As to claim 21, Suzuki et al. discloses (col. 9, line 30) that the planarizing process is a CMP processing step.

As to claim 23, Suzuki et al. discloses (col. 9, line 13) that the embedded wiring is gate wiring of a thin film transistor.

Claims 25, 26 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al.. As to claim 25, Suzuki et al., Figures 3(a) to 3(f) and 4(a) to 4(d), discloses a method for manufacturing a semiconductor device comprising the steps of: forming an insulating film (42)(col. 8, line 10)) over a substrate (10)(col. 7, line 65) having an insulating surface; forming a mask (col. 8, line 21) over the insulating film; forming a depression (43) by selectively etching the insulating film (col. 8, lines 19-22), and forming an embedded wiring, embodied initially as layer (44a), in the depression by “any known technique” (col. 8, lines 64-65). Since the disclosed electroless plating technique of Suzuki et al. uses metal in a liquid solution, it may be performed by a droplet discharge method. See, for example, Kobayashi. Suzuki et al. further discloses removing the mask; performing a planarization processing (col. 9, lines 28-30) to an upper surface of the embedded wiring; forming a gate insulating film (47)(col. 9, line 67) over the embedded wiring; and forming a semiconductor film (active layer (50), which is the same as active layer (17)(col. 5, lines 56-57)) over the gate insulating film.

As to claim 26, Suzuki et al. discloses (col. 9, line 30) that the planarizing process is a CMP processing step.

As to claim 28, Suzuki et al. discloses (col. 9, line 13) that the embedded wiring is gate wiring of a thin film transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Itagaki et al. (US 2001/0029066). Suzuki et al. discloses the method of claim 19, as described above. Suzuki et al. does not disclose expressly that the planarization processing is a heat press treatment capable of heating and pressing at the same time to perform baking of the embedded wiring. Itagaki et al., Figures 2 and 3, discloses a method (paragraph [0025]) in which heat and pressure are used to planarize a wiring layer (121) formed in an adhesive sheet. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use heat and pressure to planarize applicants wiring formed in an insulating film. The motivation for doing so would have been to obtain a level of flatness below a threshold, 10 microns in the case of Itagaki et al. (paragraph [0025]). Therefore, it would have been obvious to combine Itagaki et al. with Suzuki et al. to obtain the invention as specified in claim 22.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Yamazaki et al. (US 7,176,069). Suzuki et al. discloses the method of claim 19, as described above. Suzuki et al. does not disclose expressly that the step of forming a mask over the insulating film comprises a step of forming a first material layer and a second material layer surrounding the first material layer, wherein the first material layer is soluble in a first solvent, and wherein the second material layer is soluble in a second solvent, and wherein the first material layer and the second material layer are formed

with a device comprising a plurality of nozzles capable of discharging different materials: and a step of forming a mask comprising the first material film by removing the second material alone by the second solvent. Yamazaki et al., Figures 9A to 9D, discloses a method in which the step of forming a mask over the insulating film (10) comprises a step of forming a first material layer (11) and a second material layer (14) surrounding, in the same sense as applicants Figure 8(C), the first material layer, wherein the first material layer is soluble in a first solvent (col. 7, lines 35-39), and wherein the second material layer is soluble in a second solvent (col. 7, lines 48-49), and wherein the first material layer and the second material layer are formed with a device comprising a plurality of nozzles (13a) capable of discharging different materials: and a step of forming a mask comprising the first material film by removing the second material alone by the second solvent (col. 7, lines 48-49). At the time of invention, it would have been obvious to a person of ordinary skill in the art to use the masking and etching method of Yamazaki et al. in the device of Suzuki et al.. The motivation for doing so would have been to independently control each nozzle body by computer to selectively print or remove material (Yamazaki et al., col. 5, lines 26-35). Therefore, it would have been obvious to combine Yamazaki et al. with Suzuki et al. to obtain the invention as specified in claim 24.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Itagaki et al.. Suzuki et al. discloses the method of claim 25, as described above. Suzuki et al. does not disclose expressly that the planarization processing is a heat press treatment capable of heating and pressing at the same time to perform baking of the embedded wiring. Itagaki et al., Figures 2 and 3, discloses a method (paragraph [0025]) in which heat and pressure are used to planarize a wiring layer (121) formed in an adhesive sheet. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use heat and pressure to planarize applicants wiring formed in an insulating film. The motivation for doing so would have been to obtain a level of flatness below a threshold, 10 microns in the case of Itagaki et al. (paragraph [0025]). Therefore, it would have been obvious to combine Itagaki et al. with Suzuki et al. to obtain the invention as specified in claim 27.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Yamazaki et al.. Suzuki et al. discloses the method of claim 25, as described above. Suzuki et al. does

not disclose expressly that the step of forming a mask over the insulating film comprises a step of forming a first material layer and a second material layer surrounding the first material layer, wherein the first material layer is soluble in a first solvent, and wherein the second material layer is soluble in a second solvent, and wherein the first material layer and the second material layer are formed with a device comprising a plurality of nozzles capable of discharging different materials: and a step of forming a mask comprising the first material film by removing the second material alone by the second solvent. Yamazaki et al., Figures 9A to 9D, discloses a method in which the step of forming a mask over the insulating film (10) comprises a step of forming a first material layer (11) and a second material layer (14) surrounding, in the same sense as applicants Figure 8(C), the first material layer, wherein the first material layer is soluble in a first solvent (col. 7, lines 35-39), and wherein the second material layer is soluble in a second solvent (col. 7, lines 48-49), and wherein the first material layer and the second material layer are formed with a device comprising a plurality of nozzles (13a) capable of discharging different materials: and a step of forming a mask comprising the first material film by removing the second material alone by the second solvent (col. 7, lines 48-49). At the time of invention, it would have been obvious to a person of ordinary skill in the art to use the masking and etching method of Yamazaki et al. in the device of Suzuki et al.. The motivation for doing so would have been to independently control each nozzle body by computer to selectively print or remove material (Yamazaki et al., col. 5, lines 26-35). Therefore, it would have been obvious to combine Yamazaki et al. with Suzuki et al. to obtain the invention as specified in claim 29.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
December 15, 2008

/Evan Pert/

Primary Examiner, Art Unit 2826